Chapter 3 High-Resolution DPWM Design

As described in Chapter 2, static and dynamic output voltage regulation capabilities depend on the characteristics of the ADC resolution, the discrete set of duty ratios and ultimately the discrete set of achievable output voltages depends on the DPWM resolution. If the resolution of ADC and DPWM is not sufficiently high, an undesirable limit-cycle oscillation may occur [A7, H4, Z3]. The requirement for a high-resolution ADC and DPWM is an important consideration in the realization of digitally controlled low-power high-frequency SMPS. Thanks to the advanced CMOS technologies and the windows ADC techniques, the challenge of speed and resolution of ADC is becoming a less important issue. Because the final ASIC implementation of the full digital controller is not available in the time of this work (before April 2009), Thus the ADC design is not discussed in the dissertation and practical validations are performed with FPGA and discrete ADCs.

High resolution DPWM is then the key module to restrain the undesired limit cycle. Several alternative solutions have been proposed in recent years for high-resolution low-power DPWM architectures reviewed in Chapter 2, such as the hardware methods: delay-line, hybrid delay-line, segment delay-line, ring oscillator, segment ring-oscillator and Delay Locked Loop (DLL), and the soft methods: digital dither and Δ-Σ modulator. These architectures can increase DPWM resolution to some extent, however they either entirely rely on hardware method such as the most advanced and expensive CMOS technologies for tight delay-cell/ or ring-oscillator, or completely depend on soft method such as digital dither and Δ-Σ modulator.

In order to increase resolution and reduce power consumption simultaneously, the soft methods and hardware resources should be fully utilized as furthest as possible. Based on the advantage of DCM (Digital Clock Management) phase-shift [M3] characteristics available on FPGA resources, in this work we propose two hybrid 11-bit DPWMs which associate with digital dithering [A7] and Δ-Σ modulator[R6, D2] respectively. One is the hybrid dither DPWM which includes a 3-bit digital dithering approach, a 4-bit DLL phase-shift block and a 4-bit counter comparator. The other is the hybrid Δ-Σ DPWM which contains a 5-bit multi-stage Δ-Σ modulator, a 4-bit DLL phase-shift block and a 2-bit counter comparator.
3.1 Design of a 11-bit Hybrid Dither DPWM

The idea of the hybrid dither DPWM architecture is to take the advantage of the combination of hardware method (counter comparator and DLL phase-shift) and soft method (digital dither) to alleviate the requirement of high frequency clock and reduce power consumption. The proposed FPGA-based DPWM includes three blocks: 3-bit digital dithering approach, 4-bit segmented DCM phase-shift and 4-bit counter comparator. As a consequent, for operation at switching frequency \( f_s \), the counter comparator block merely needs a \( 2^4 f_s \) clock instead of the \( 2^{11} f_s \), which dramatically alleviates the high clock frequency requirement.

Fig. 3-1 shows the schematic diagram of the hybrid dither DPWM. Each block will be detailed in next sub-sections.

3.1.1 Design of a 3-bit digital dither block

A. Principle of Digital Dither Approach

Analog dither has proved its efficiency for increasing the resolution of a PWM module [S3]. However it is difficult to generate and control as analog dither is sensitive to variations of analog component values and it can only be mixed with analog signals in the converter and not with signals inside a digital controller. On the contrary digital dither [A7] can be generated inside the digital controller and it is easier to implement and control. Moreover it does not suffer from the problem of component value variations. It is designed in a straightforward manner in a FPGA using digital logic circuits.

The basic principle of digital dither is detailed in [A7]. It consists to distribute the \( N_{dith} \) LSB of the duty value as 1-bit value of “0” or “1” in a pre-scheduled sequence, and put the specific LSB effects into hardware \( N_{core} \) MSB during an averaging process. The \( (N_{core} + N_{dith}) \) bits duty value from control law will be modified in an averaging distribution over \( 2^{N_{dith}} \) switching cycles, so that the equivalent duty value is shaped in the value range of \( 2^{N_{dith}} \) adjacent quantized levels. By using dither method, the hardware \( N_{core} \) bits DPWM
can be increased by $N_{\text{dither}}$ bits:

$$N_{\text{DPWM}} = N_{\text{Core}} + N_{\text{dither}}$$  \hspace{1cm} (3-1)$$

where $N_{\text{DPWM}}$ is equivalent as the DPWM effective bit number. By using dither methods, the LSB bit of the duty value is alternating between “0” and “1” in a specific look-up table pattern during the $2^N_{\text{dith}}$ switching cycles. As a result, the effective DPWM resolution can be increased by $N_{\text{dither}}$ bits. Fig. 3-2 shows the general schematic diagram of digital dither implementation, where $f_s$ is switching frequency. In order to avoid poor output regulation and limit cycles, a rectangular-waveform [A7] dither pattern (shown in Fig. 3-3) is adopted.

![Fig. 3-2 Structure for adding arbitrary dither patterns to the duty cycle](image)

For instance of a 2-bit dither approach, Fig. 3-3 shows how the dither schema realizes the digital dithering during $2^2$ duty cycles and Table 3-1 shows the dithering pattern [A7], where $D_{c1}$ and $D_{c2}$ are two adjacent initial quantized levels with $D_{c2} = D_{c1} + \text{LSB}$. It can be seen that when the duty value changes between $D_{c1}$ and $D_{c2}$ in a dither sequence during every $2^2$ switching periods, a corresponding sub-bit level can be implemented by averaging over 4 switching cycles.

![Fig. 3-3 Scheme of 2-bit rectangular-waveform dither pattern](image)

<table>
<thead>
<tr>
<th>2-bit LSB (line index)</th>
<th>$2^2$ switching cycles (row index)</th>
<th>Sequence average</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>0 0 0 0</td>
<td>0</td>
</tr>
<tr>
<td>01</td>
<td>0 0 0 1</td>
<td>1/4</td>
</tr>
<tr>
<td>10</td>
<td>0 1 0 1</td>
<td>1/2</td>
</tr>
<tr>
<td>11</td>
<td>0 1 1 1</td>
<td>3/4</td>
</tr>
</tbody>
</table>

![Table 3-1 2-bit digital dithering look-up table](image)
The dither method has advantages such as simple and easy implementation, and high DPWM resolution can be achieved in high switching frequency without increasing the clock frequency and power consumption. However, dither comes not free. The dithering of the duty value results in duty ratio error and increases additional AC ripple at the output LC filter. Considering the instance above, when the 11-bit duty ratio changes from 0.500244 to 0.503664 by 1-bit LSB per switching cycle, the dithering schema and look-up table for the 3-bit dither pattern are shown in Fig. 3-4 and Table 3-2 respectively. The comparison of dithering results between 2-bit dithering and 3-bit dithering are respectively shown in Table 3-3 and Table 3-4. It can be seen that the duty ratio error (shadow area) of 3-bit dither pattern is two times that of 2-bit dither pattern, and the duty ratio error will increase by double per 1-bit augment in dither. It is clear that the longer bits the dither patterns used, the larger the duty ratio error (i.e. the larger the AC ripple). The higher output ripple increases and sub-harmonic may occur, which may cause EMI problem during the operation. Thus this consideration puts a practical limit on the number of dither bits that can be added to increase the resolution of the DPWM.

![Fig. 3-4 Scheme of 3-bit rectangular-waveform dither pattern](image)

<table>
<thead>
<tr>
<th>3-bit LSB (line index)</th>
<th>2^2 switching cycles (row index)</th>
<th>Sequence average</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>0 0 0 0 0 0 0 0 0 0 0 0</td>
<td>0</td>
</tr>
<tr>
<td>001</td>
<td>0 0 0 0 0 0 0 0 0 1 0 0</td>
<td>1/8</td>
</tr>
<tr>
<td>010</td>
<td>0 0 0 1 0 0 0 0 1 0 0 0</td>
<td>2/8</td>
</tr>
<tr>
<td>011</td>
<td>0 0 1 0 0 1 0 1 0 1 0 0</td>
<td>3/8</td>
</tr>
<tr>
<td>100</td>
<td>0 1 0 1 0 1 0 1 0 1 0 1</td>
<td>4/8</td>
</tr>
<tr>
<td>101</td>
<td>0 1 0 1 0 1 0 1 0 1 0 1</td>
<td>5/8</td>
</tr>
<tr>
<td>110</td>
<td>0 1 1 1 0 1 1 1 1 1 1 1</td>
<td>6/8</td>
</tr>
<tr>
<td>111</td>
<td>0 1 1 1 1 1 1 1 1 1 1 1</td>
<td>7/8</td>
</tr>
</tbody>
</table>
Table 3-3 A 11-bit digital dithering in 2-bit pattern

<table>
<thead>
<tr>
<th>2-LSB counter</th>
<th>desired duty value (11-bit)</th>
<th>desired duty ratio</th>
<th>Dither value</th>
<th>actual duty value (9-bit)</th>
<th>actual duty ratio</th>
<th>duty ratio error</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>100000000000</td>
<td>0.500244</td>
<td>0</td>
<td>100000000</td>
<td>0.500979</td>
<td>0.0735%</td>
</tr>
<tr>
<td>1</td>
<td>100000000001</td>
<td>0.500733</td>
<td>1</td>
<td>1000000001</td>
<td>0.502935</td>
<td>0.2202%</td>
</tr>
<tr>
<td>2</td>
<td>100000000010</td>
<td>0.501221</td>
<td>1</td>
<td>1000000001</td>
<td>0.502935</td>
<td>0.1714%</td>
</tr>
<tr>
<td>3</td>
<td>100000000011</td>
<td>0.501710</td>
<td>1</td>
<td>1000000001</td>
<td>0.502935</td>
<td>0.1225%</td>
</tr>
<tr>
<td>0</td>
<td>100000001000</td>
<td>0.502198</td>
<td>1</td>
<td>1000000010</td>
<td>0.504892</td>
<td>0.2694%</td>
</tr>
<tr>
<td>1</td>
<td>100000001010</td>
<td>0.502687</td>
<td>1</td>
<td>1000000010</td>
<td>0.504892</td>
<td>0.2205%</td>
</tr>
<tr>
<td>2</td>
<td>100000001100</td>
<td>0.503175</td>
<td>1</td>
<td>1000000010</td>
<td>0.504892</td>
<td>0.1717%</td>
</tr>
<tr>
<td>3</td>
<td>100000001111</td>
<td>0.503664</td>
<td>1</td>
<td>1000000010</td>
<td>0.504892</td>
<td>0.1228%</td>
</tr>
</tbody>
</table>

Table 3-4 A 11-bit digital dithering in 3-bit pattern

<table>
<thead>
<tr>
<th>3-LSB counter</th>
<th>desired duty value (11-bit)</th>
<th>desired duty ratio</th>
<th>Dither value</th>
<th>actual duty value (8-bit)</th>
<th>actual duty ratio</th>
<th>duty ratio error</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>100000000000</td>
<td>0.500244</td>
<td>0</td>
<td>100000000</td>
<td>0.501961</td>
<td>0.1717%</td>
</tr>
<tr>
<td>1</td>
<td>100000000001</td>
<td>0.500733</td>
<td>1</td>
<td>100000001</td>
<td>0.505882</td>
<td>0.5149%</td>
</tr>
<tr>
<td>2</td>
<td>100000000010</td>
<td>0.501221</td>
<td>1</td>
<td>100000001</td>
<td>0.505882</td>
<td>0.4661%</td>
</tr>
<tr>
<td>3</td>
<td>100000000011</td>
<td>0.501710</td>
<td>1</td>
<td>100000001</td>
<td>0.505882</td>
<td>0.4172%</td>
</tr>
<tr>
<td>4</td>
<td>100000001000</td>
<td>0.502198</td>
<td>1</td>
<td>1000000010</td>
<td>0.505882</td>
<td>0.3684%</td>
</tr>
<tr>
<td>5</td>
<td>100000001010</td>
<td>0.502687</td>
<td>1</td>
<td>1000000000</td>
<td>0.505882</td>
<td>0.3195%</td>
</tr>
<tr>
<td>6</td>
<td>100000001100</td>
<td>0.503175</td>
<td>1</td>
<td>1000000000</td>
<td>0.505882</td>
<td>0.2707%</td>
</tr>
<tr>
<td>7</td>
<td>100000001111</td>
<td>0.503664</td>
<td>1</td>
<td>10000000001</td>
<td>0.505882</td>
<td>0.2218%</td>
</tr>
</tbody>
</table>

B. Determine the Bit Number of Dither

In order to determine how many bits can be used under the maximum peak-to-peak voltage ripple $V_{p-p\_dither}$ produced by dither in rectangular-waveform dither pattern, some useful mathematical analysis (see [A7] for details) can give an estimate of the relation between maximum peak-to-peak voltage ripple $V_{p-p\_dither}$ produced by the dither and the number of dither bits $N_{dith}$.

For $f_c < f_{dith} < f_z$:

$$V_{p-p\_dither} \leq \left( \frac{f_c}{f_s} \right)^2 \frac{2^{2N_{dith}}}{\pi} \frac{4V_{in}}{2^{N_{Core}}} \quad (3-2)$$

And for $f_c < f_z < f_{dith}$:

$$V_{p-p\_dither} \leq \left( \frac{f_z}{f_s} \right)^2 \left( \frac{f_{dith}}{f_s} \right) \frac{2^{2N_{dith}}}{\pi} \frac{4V_{in}}{2^{N_{Core}}} \quad (3-3)$$

Where $f_s$ is the switching frequency, $N_{dith}$ is the bit number of dither, $N_{Core}$ is the bit number of hardware DPWM, $V_{in}$ is the input voltage, $f_c$ is the LC filter cut-off frequency,
\[ f_c = \frac{1}{2\pi \sqrt{LC}} \]  
(3-4)

\[ f_c \] is the ESR zero frequency associated with the output capacitor,

\[ f_c = \frac{1}{2\pi R_{ESR}C} \]  
(3-5)

and the dither waveform with the largest low frequency component is a square wave with 50% duty ratio at frequency \( f_{dith} \)

\[ f_{dith} = \frac{f_c}{2^{N_{dith}}} \]  
(3-6)

Once the amplitude of the dither \( V_{pp-dither} \) is known, we can develop a condition on how many bits of dither, \( N_{dith} \), can be used in a certain system without inducing limit cycles. To ensure that the dither does not cause steady-state limit cycling, the DPWM should always be an effective level that completely fits into one ADC quantization bin, taking into account the dither ripple. With \( N_{dith} \) bit dither, the effective DPWM quantization bin size

\[ \Delta V_{DPWM} = V_{in} / 2^{N_{new}} = V_{in} / 2^{N_{Core} + N_{dith}} \]  
(3-7)

Assuming that the smallest dither ripple amplitude is when the DPWM levels are located at one DPWM bin size (with two boundaries: upper and bottom) from the center of the ADC bin. Then the tolerable peak-to-peak dither ripple amplitude is bounded by

\[ \frac{1}{2} V_{pp-dither} \leq (\Delta V_{ADC} - \Delta V_{DPWM}) \]  
(3-8)

Where \( \Delta V_{ADC} \) is ADC quantization bin size,

\[ \Delta V_{ADC} = V_{in} / 2^{N_{ADC}} = V_{in} / 2^{N_{new} - \Delta N} = V_{in} / 2^{N_{Core} + N_{dith} - \Delta N} \]  
(3-9)

Where \( \Delta N \) is the difference-bit number between DPWM quantization \( N_{DPWM} \) and ADC quantization \( N_{ADC} \),

\[ \Delta N = N_{DPWM} - N_{ADC} = (N_{Core} + N_{dith}) - N_{ADC} \]  
(3-10)

As mentioned in section 2.1.2, it was suggested that making the resolution of the DPWM one bit larger than that of the ADC adequately satisfies the condition to eliminate steady-state limit cycling, hence the minimum \( \Delta N \geq 1 \). Substituting equation (3-7) and (3-9) and (3-10) into (3-8),

\[ \frac{1}{2} V_{pp-dither} \leq V_{in} \left( 2^{\Delta N - 1} \right) / 2^{N_{new}} \]  
(3-11)

Combining equation (3-11) with (3-2) and (3-3), we can obtain a bound on \( N_{dith} \) (takes the upper rounded integer value of the product):

For \( f_c < f_{dith} < f_c \):
\[ N_{dith} \leq \frac{1}{2} \log_2 \left[ \pi \left( \frac{f_z}{f_c} \right)^2 \frac{2^{N_{Core}}}{2^{N_{Core}} - 1} \right] \]  

(3-12)

And for \( f_c < f_z < f_{dith} \):

\[ N_{dith} \leq \frac{1}{2} \log_2 \left[ \pi \left( \frac{f_z}{f_c} \right)^2 \frac{2^{N_{Core}}}{2^{N_{Core}} - 1} \right] \]  

(3-13)

C. 3-bit Digital Dither Block

When the digital dither approach is applied to the 11-bit DPWM architecture, the bit number of dither can be determined using those useful mathematical analysis [A7] mentioned above part B. The parameters of buck converter are: \( C = 22\mu F, R_{ESR} = 10\, \Omega, L = 4.7\mu H, f_s = 2\, MHz, N_{DPWM} = 11\)-bit, \( N_{Core} = 8\)-bit, \( \Delta N = 1 \) and \( V_{in} = 3.3\, V \). According to equation (3-4), (3-5) and (3-6), then \( f_c = \frac{1}{2}\left(2\pi\sqrt{LC}\right) = 0.01565\times10^6 \) and \( f_z = \frac{1}{2}\left(2\pi R_{ESR}C\right) = 0.90429\times10^6 \). The maximum peak-to-peak voltage ripple produced by dither can be estimate by equation (3-11):

\[ V_{p-p, dither} \leq 2 \times V_{in} \left(2^{\Delta N} - 1\right) / 2^{N_{Core}} = 3.2\, mV \]  

(3-14)

The range of bit number of dither \( N_{dith} \) can be determined by equation (3-6): 1.487 < \( N_{dith} < 11.305 \) for the condition \( f_c < f_{dith} < f_z \) and \( N_{dith} < 1.487 \) for the condition \( f_c < f_{dith} < f_z \). It should be noted that \( 1 \leq N_{dith} \), thus the dither frequency fits the condition \( f_c < f_{dith} < f_z \). Consequently the maximum bit number of dither can be obtained by (3-12):

\[ N_{dith} \leq \frac{1}{2} \log_2 \left[ \pi \left( \frac{f_z}{f_c} \right)^2 \frac{2^{N_{Core}}}{2^{N_{Core}} - 1} \right] = \frac{1}{2} \log_2 \left[ \pi \left( \frac{2 \times 10^6}{0.90429 \times 10^6}\right) \right] = 4.8234 \]  

(3-15)

which means that the bit number of dither should be limited \( N_{dith} < 4.8234 \) to satisfy the tolerant voltage ripple (3.2 mV). Thus the bit number of dither can be adapted from 2 to 4 in this case. Here we use a 3-bit digital dithering pattern in the 11-bit hybrid DPWM.

The operations of the 3-bit dither pattern are already shown in Fig. 3-4 and Table 3-2 respectively. Fig. 3-5 shows the implementation of the 3-bit proposed digital dithering block. The obtained 8-bit duty \( D[7:0] \) will be implemented by the hardware Core DPWM (a 4-bit counter-comparator and a 4-bit segmented DCM phase-shift block).

![Fig. 3-5 The diagram block of proposed 3-bit digital dithering](image-url)
3.1.2 Design of a 4-bit Segmented DCM Phase-Shift Block

Digital Clock Manager (DCM) functionality block is available in most digital FPGA devices. It includes the general DLL (Delay-Locked Loop) and/or PLL (Phase-Locked Loop) modules, which can not only produce multi synchronous clocks with zero propagation delay, but also offer multi asynchronous clocks with low skew phase-shift. Virtex-II FPGA provides advanced DCM clocking capabilities to optionally multiply and divide the incoming clock frequency to synthesize a new clock frequency [X2]. DCM shifts the clock phase optionally to delay the incoming clock by a fraction of the clock period. For instance shown in Fig. 3-6, the DCM divides the incoming clock $F_{CLK}$ (50% ratio) into four equal clocks $clk_0$, $clk_90$, $clk_180$ and $clk_270$ respectively, then the four phase-shifted clocks can act as an equivalent $2^2 \times F_{CLK}$ clock with a 4:1 multiplexer. Thus the clock for the DCM architecture can be reduced by $2^2$ times for a fixed-resolution DPWM, or the resolution can be increased by $2^2$ bits for a fixed-frequency DPWM. Since the relationship between system clock $F_{CLK}$, hardware Core DPWM resolution $N_{Core}$ and switching frequency $f_s$ can be written as:

$$F_{CLK} = 2^{N_{Core}} \cdot f_s$$

(3-16)

Then the required clock $F_{DCM}$ for the four-phase-shift DCM module can be expressed as:

$$F_{DCM} = F_{CLK} \cdot 2^{(N_{DCM}-2)} = \left(2^{N_{Core}+N_{DCM}-2}\right) \cdot f_s$$

(3-17)

where $N_{DCM}$ is the bit number of DPWM implemented by four-phase-shift DCM module.

![Fig. 3-6 DCM four-phase-shift scheme](image)

Based on the advantage of DCM phase-shift module, a segmented DCM phase-shift architecture which uses two DCM phase-shift modules in series for digital clock application was introduced in [M3]. This segmented DCM architecture is employed as a 4-bit DPWM block of high-frequency digital control in our work.

The proposed DPWM including a 4-bit counter comparator, then the hardware clock frequency $F_{CLK} = 2^4 f_s$. According to equation (3-17), the incoming clock frequency $F_{DCM}$ for

41
the segmented DCM module, \( F_{DCM} = F_{CLK} \cdot 2^{(4+4-2)} = 2^6 \cdot F_{CLK} \). The diagram block of the 4-bit segmented DCM phase-shift architecture is shown in Fig. 3-7, where the input clock \( F_{CLK} \) propagates in zero delay through the first DCM block, \( DCM-I \) in this case, and the first phase shifted versions, \( PX0, PX90, PX180 \) and \( PX270 \), are generated. The clock \( F_{DCM} \), four times incoming clock \( F_{CLK} \), is operated at the second DCM block, \( DCM-II \), and further phase shifted signals of the clock are produced, \( PY0, PY90, PY180 \) and \( PY270 \). As observed from Fig. 3-7, the resolution is now increased by 16 times without the need of operating the whole system at 16 times higher \( F_{CLK} \).

Using two multiplexers to select the corresponding shifted clock signals, the whole block realizes the 4-bit DPWM duty \( D[3:0] \) from digital dithering block. Depending on duty value \( D[3:2] \), \( S_1 \) can be derived from the one of four phase-shifted clock signals \( PX0, PX90, PX180 \) and \( PX270 \). The selected \( S_1 \) acts as an equivalent clock of four times (x4) the phase-shifted signals. Similarly, duty value \( D[1:0] \) selects one of the four phase-shifted clock signals \( PY0, PY90, PY180 \) and \( PY270 \) for \( S_2 \) which acts an equivalent clock of four times (x4) the phase-shifted signals. Then the two selected signals are operated in logic AND circuit to generate the final phase-shift signal \( S_c \) which has 16 times (double x4) incoming \( F_{CLK} \) and will be sent to counter comparator. The most attractive merit for this segmented DCM phase-shift architecture is that the final output signal \( S_c \) has \( 2^4 \) kinds of clock possibilities during each of \( F_{CLK} \) clock cycle, where \( S_1 \) has \( 2^2 \) kinds of “coarse” phase-shift and \( S_2 \) has \( 2^2 \) kinds of “fine” phase-shift. Thus this segmented DCM block can either increase 4-bit DPWM resolution (for fixed \( f_s \)) or increase the switching frequency by \( 2^4 \) times (for fixed \( N_{DPWM} \)). The operation waveforms of the 4-bit segmented DCM phase-shift module are shown in Fig. 3-8.
3.1.3 Design of a 4-bit Fast Counter-Comparator Block

Fast counter-comparator is one simple hardware method to achieve digital-to-time conversion in Core DPWM. This architecture uses a cycling counter and a comparator, setting a set-reset (SR) latch high when the counter value is zero and low when the counter reaches the control duty value $D$. This scheme has the advantage of a simple structure and an excellent linearity in the digital to time-domain-conversion. According to equation (3-16), it needs $2^N f_s$ clock to achieve an $N$-bit DPWM at switching frequency $f_s$. However when operating at the high frequency $f_s$, it falls into the drawback of very high power consumption. Thus the fast counter-comparator is usually used as the solution for the implementation of few MSB rather than a whole DPWM architecture.

Linking to the 3-bit digital dithering and 4-bit segmented DCM phase-shift blocks above; a 4-bit counter-comparator block shown in Fig. 3-9 is adopted in this hybrid DPWM. It includes a 4-bit counter, a 4-bit comparator and a FDP (D Flip-Flop with Asynchronous Preset). Where $D[7:4]$ and $S_c$ respectively come from the 3-bit digital dithering block and the 4-bit DCM phase-shift block. An example is employed to explain the operation for the 4-bit counter-comparator block, where $D[7:4]="1010"$ and $D[3:0]="1011"$, the operation waveforms are shown in Fig. 3-10.

![Fig. 3-8 Operation waveforms of the 4-bit segmented DCM phase-shift module](image-url)
3.1.4 Operation of the Hybrid Dither DPWM

Taking a combination of three blocks described above: 3-bit digital dithering, 4-bit DCM phase-shift and 4-bit counter comparator, the completed DPWM can be figured in Fig. 3-11.

The operation procedure of the DPWM is described as follows: The duty value \( d \) is generated by the digital control law in 11-bit and varies from the minimum value \( d[00000000000] \) (0) to the maximum value \( d[11111111111] \) (2047), which is sent to DPWM architecture at beginning of each switching cycle. Initially the 11-bit duty value \( d \) goes into

![Diagram of the 4-bit counter-comparator block](image)

![Operation waveforms of the 4-bit counter comparator block](image)

![Diagram of the proposed 11-bit hybrid dither DPWM](image)
**digital dithering** block, where the 3-LSB \(d[2:0]\) acts as the line index and the 3-bit counter value indicates the row index in the look-up table (shown in Fig. 3-4 and Table. 3-2). Then a 1-bit dither value is acquired and added to duty ratio MSB \(d[10:3]\) in an 8-bit saturated adder, where a new 8-bit duty ratio \(D[7:0]\) is generated. For the new duty \(D\), the MSB \(D[7:4]\) are delivered to the 4-bit \textit{counter-comparator} block and the LSB \(D[3:0]\) are assigned for the 4-bit \textit{segmented DCM phase-shift} block. The selected signals \(S_c\) (from \textit{segmented DCM phase-shift} block) and \(S_k\) (from \textit{counter-comparator} block) are operated by logic AND circuit, resulting in another signal \(R_{set}\). The signals \(S_{set}\) and \(R_{set}\) respectively connect to the ports \(PRE\) and \(C\) of the FDP logic circuit to change the PWM states ON/OFF. For instance, supposing that the duty value from the control algorithm is \(d[01010101010]\) and the 3-bit counter value in digital dithering block is “010”. According to Table 3-2, the 1-bit dither value ‘1’ will be added to \(d[10:4]\) by a saturated adder resulting in a new duty \(D[01010110]\). The \(D[7:4]\) (“0101”) is implemented by the 4-bit \textit{counter-comparator}, \(D[3:2]\) (“01”) is used to select phase-shifted clock \(PX90\) for signal \(S_1\), and \(D[1:0] = ”10”\) is set to select phase-shifted clock \(PY180\) for \(S_2\). Through the logic AND operation of \(S_1\) and \(S_2\), the final phase-shifted signal \(S_C\) is obtained and sent to FDP to change PWM signal. The logic waveforms for the example operation are shown in Fig. 3-12.

![Logic waveforms for the example operation of 11-bit hybrid dither DPWM](image)

Fig. 3-12 Logic waveforms for the example operation of 11-bit hybrid dither DPWM

In the FPGA implementation, the 11-bit DPWM signal with 2MHz switching frequency is realized by the proposed hybrid DPWM, where 3-bit are implemented by \textit{digital dithering} (\(N_{dith} = 3\)), 4-bit are achieved by \textit{segmented DCM phase-shift} block (\(N_{DCM} = 4\)), and 4-bit are generated by \textit{counter-comparator} (\(N_{Core} = 4\)). According to equations (3-16) and (3-17) respectively, the FPGA system clock is \(F_{CLK} = 2^4 f_s\) and the clock signal shifted in DCM module is \(F_{DCM} = 2^2 F_{CLK} = 2^6 f_s\). When operating at \(f_s = 2\text{MHz}\) the \(F_{CLK}\) is merely 32MHz, which dramatically alleviates the system clock requirement and reduces the power.
consumption of DPWM. For example, when a 11-bit DPWM operating at 2MHz in the digital dithering approach [A7] or in the segmented DCM phase-shift [M3], respectively, the $F_{CLK}$ will be required $2^8 f_s = 512$MHz or $2^7 f_s = 256$MHz. By contrast, the proposed hybrid dither DPWM can allow operation at higher switching frequency with lower power consumption.

The implementation of the proposed 11-bit hybrid DPWM is performed on a XC2VP30 FPGA and the simulation is verified in post-placed route using Xilinx ISE9.2 tool. The single four-phase-shift DCM functionality shown in Fig. 3-6 is verified and the timing-waveform is shown in Fig. 3-13. The timing-simulation results for the segmented DCM phase-shift shown in Fig. 3-7 are figured in Fig. 3-14, where $f_s=2$MHz, $F_{DCM} = 128$MHz, $F_{CLK} = 32$MHz and the duty ratio 50% with $D[7:0] = “10000000”$. Finally the timing-simulation waveforms of the complete 11-bit hybrid DPWM shown in Fig. 3-11 is illustrated in Fig. 3-15 with an example duty value $D[7:0] = “10000111”$. The experimental tests of the hybrid DPWM based on a discrete buck converter will be detailed in Chapter 6.
low-skew DLL/and PLL design. The technique of designing a similar DLL IP Core in ASIC is not a critical issue in IC design. This issue is not discussed here.

3.2 Design of a 11-bit Hybrid MASH Δ-Σ DPWM

Section 3.1 describes an 11-bit hybrid dither DPWM which can operate up to 2MHz switching frequency in FPGA-implementation. The most valuable advantage of the DPWM is that the hybrid architecture can dramatically alleviate the requirement of high clock frequency and consequently reduce the power consumption. For operation of 11-bit DPWM at 2MHz, it merely requires a system clock 32MHz (128MHz for DCM block only).

Like the method digital dither, another one practical soft method to increase effective resolution of DPWM is Delta-Sigma (Δ-Σ) modulator, which is based on the well known noise-shaping technology [R6, Y4, S10, D2]. As an alternative, it is very interesting to employ a Δ-Σ modulator to increase the resolution and reduce power consumption for DPWM.

3.2.1 MASH Δ-Σ Modulator Design

A. Principle of Δ-Σ modulator

Delta-Sigma (Δ-Σ) has been widely used in analog-to-digital and digital-to-analog conversion. It is based on the well-known noise-shaping concept which can be fabricated in low-cost CMOS technologies [R6, D2]. Fig. 3-16 shows the general structure of a signal-quantizer Δ-Σ modulator, where Loop Filter is to process the input signal by noise-shaping modulator that generally is a delay or integrator block, $E$ is the noises, $Q$ is the quantizer and $V$ is the output signal. For a first order Δ-Σ, the modulator can be transformed into a detailed linear model in z-domain as shown in Fig. 3-17.
From the diagram, it can be written:

\[ Y(z) = z^{-3}Y(z) + U(z) - z^{-1}V(z) \]  

(3.18)

Thus

\[ V(z) = Y(z) + E(z) \]

\[ = z^{-1}Y(z) + U(z) - z^{-1}V(z) + E(z) = U(z) + z^{-1}\left[ Y(z) - V(z) \right] + E(z) \]  

(3.19)

Then

\[ V(z) = U(z) + (1 - z^{-1})E(z) \]  

(3.20)

Equation (3.20) can be rewritten in the digital signal process form

\[ V(z) = STF(z) \cdot U(z) + NTF(z) \cdot E(z) \]  

(3.21)

where \( STF \) is the signal transfer function which is unity here, \( STF(z) = 1 \), and \( NTF \) is the noise transfer function with \( NTF(z) = (1 - z^{-1}) \). In steady-state, when the \( \Delta \Sigma \) loop has infinite gain at zero frequency, i.e., \( z \approx 1 \) and consequently \( ||NTF(z)|| \ll 1 \), it suppresses the quantization noise at and near dc component. Therefore the \( \Delta \Sigma \) modulator can dramatically eliminate the quantization noise and then the input signal can be well remained,

\[ V(z) \rightarrow U(z) \]  

(3.22)

Similarly a second-order \( \Delta \Sigma \) modulator can be transformed to a detailed linear model in \( z \)-domain shown in Fig. 3-18.
From the schema, the output signal $V(z)$ can be written:

$$V(z) = E(z) + \frac{-z^{-1}V(z)}{(1-z^{-1})} + \frac{-z^{-1}V(z) + U(z)}{(1-z^{-1})^2}$$  \hspace{1cm} (3.23)

Through simplification

$$V(z) = U(z) + (1 + z^{-1})^2 \cdot E(z)$$  \hspace{1cm} (3.24)

Rewritten in the digital signal process form of (3.21), here $STF = 1$ and $NTF = (1-z^{-1})^2$.

### B. Δ-Σ Modulator Application in DPWM

For the DPWM application in Δ-Σ digital signal process, the loop architecture function is similar to that of the noise-shaping loop in application of analog-to-digital and digital-to-analog, namely to reduce the resolution of the large-bit input signal to a few-bit value without significant quantization error-bit in the process. An architecture configuration for Δ-Σ DPWM is illustrated in Fig. 3-19 (a), where the discarded LSBs (error $e(n)$) are filtered and fed-back to the input port. The filter $He$ generally is a delay or integrator block. To simplify the DPWM schematic diagram, the process “Limit” and “Truncate” can be incorporated as a “Truncation” block shown in Fig. 3-19 (b).

From Fig. 3-19, the transfer function in the linear model is given by

$$V(z) = Y(z) + E(z)$$  \hspace{1cm} (3.25)

where $E(z)$ is the quantization error of truncation, and $Y(z)$ can be expressed as:

$$Y(z) = U(z) + He(z) \cdot E(z) - He(z) \cdot V(z)$$  \hspace{1cm} (3.26)

Thus equation (3.25) can be rewritten:

$$V(z) = U(z) + He(z) \cdot Y(z) - He(z) \cdot V(z) + E(z)$$

$$= U(z) + [1 - He(z)] \cdot E(z)$$  \hspace{1cm} (3.27)

Assuming that the filter $He$ is a delay, $z^{-1}$, equation (3.27) is identical to (3.20), which demonstrates that the Δ-Σ modulator can be applied in DPWM as well as in ADC and DAC.

From the equation (3.27), it can be seen that $STF = 1$, and $NTF = 1 - He(z)$ in digital signal process. This equation shows how the transfer function $NTF$ influences the truncated...
signal. When the loop filter has infinite gain ($|H_e| \approx 1$) at zero frequency, the noise can be eliminated dramatically ($||NTF(z)|| << 1$). Therefore the high-resolution PWM input signal is almost unchanged, the quantization error is suppressed, and consequently the output PWM signal becomes approximately equal to the input PWM signal.

Although the Δ-Σ noise-shaping modulator is not new in IC design for ADC, it has not yet been widely used in recent booming digital PWM control. As far as the relevant literature, two Δ-Σ DPWM modulators have been proposed in digitally controlled high-frequency low-power SMPS by Z. Lukic et al. The first Δ-Σ DPWM was proposed in 2005 [Z2], where a first-order Δ-Σ DPWM was adopted (shown in Fig. 3-20 (a)). The other was proposed in 2007 [Z1], where a second-order Δ-Σ DPWM was presented (shown in Fig. 3-20 (b)).

![Fig. 3-20 A first-order Δ-Σ DPWM (a) and a second-order Δ-Σ DPWM (b)](image)

Although the low-order Δ-Σ DPWM has the advantages of simplicity, robustness, stability and ease for realization, the noise-shaping performance of this DPWM is still limited such as it has the potential problems of low-frequency tones and slow convergence [Z1, R6, S10]. By contrast, the high-order Δ-Σ architecture has higher noise-shaping performance such that can strongly suppress low-frequency tones and have faster convergence [R6, D2]. However as a contradictory term with noise-shaping performance, the stability must be considered in the design for high-order error-feedback loop.

As illustrated in equation (3-20) and described in previous part $A$, since $STF$ acts essentially like a pre-filter, the stable input range of a Δ-Σ modulator is primarily determined by $NTF$ and the bit number of the quantizer. However due to absence of standard criterion for $NTF$ properties that are necessary and sufficient for stable operation, it is difficult to exactly analyze the stability of a high-order Δ-Σ modulator [D2]. Especially it has no solid theoretical foundations to estimate the stability of a multi-bit-signal DPWM. Evidently high-order Δ-Σ may cause the potential instability problem, however it is hard to evaluate the performance of stability and it needs to be conformed by extensive simulation and experimental results [R6].
C. Proposed MASH Second-Order DPWM

A different structure which eases the stability problem in high-order Δ-Σ is the cascade modulator, also called the Multi-stAage-noise-SHaping (MASH) modulator [R6, D2]. The basic concept of the MASH (two-stage) Δ-Σ is illustrated in Fig. 3-21.

Where Loop Filter is noise-shaping modulator that generally is a delay or integrator block, $E$ is the noises of quantizer, $Q$ is the quantizer and $V$ is the output signal. The output signal of the first-stage is given by:

$$V_1(z) = STF_1(z) \cdot U(z) + NTF_1(z) \cdot E_1(z)$$  \hspace{1cm} (3.28)

where $STF_1$ and $NTF_1$ are the signal transfer function and the noise transfer function of the first-stage loop respectively. The output signal of the second-stage is given by

$$V_2(z) = STF_2(z) \cdot E_1(z) + NTF_2(z) \cdot E_2(z)$$  \hspace{1cm} (3.29)

where $STF_2$ and $NTF_2$ are the signal transfer function and the noise transfer function of the second-stage loop respectively. The digital filter stages $H_1$ and $H_2$ at the outputs of the two loops are designed such that in the overall output $V(z)$ of the system, the first-stage error $E_1(z)$ is cancelled by setting [R6]:

$$H_1 \cdot NTF_1 - H_2 \cdot STF_2 = 0$$  \hspace{1cm} (3.30)

Usually the choice for $H_1$ and $H_2$ which satisfies the above equation is $H_1 = k \cdot STF_2$ and $H_2 = k \cdot NTF_1$, where $k$ is a constant chosen to give unity signal gain and $STF_2$ is often a delay $z^{-1}$. For easy discussion in this case, let $k = 1$ and the overall output is then given by

$$V(z) = H_1 \cdot V_1(z) - H_2 \cdot V_2(z) = STF_2 \cdot STF_1 \cdot U(z) - NTF_1 \cdot NTF_2 \cdot E_2(z)$$  \hspace{1cm} (3.31)

In practical implementation, both stages of the MASH Δ-Σ may contain a first-order or a second-order loop.
Compared with the single-stage $\Delta$-Σ modulator such as first-order \([Z2]\), \([A11]\), and second-order one \([Z1]\), the MASH structure shown in Fig. 3-21 has the advantages that makes it possible to use low-distortion loop filter in all stages to obtain the first-stage error $e_1(n)$ without any subtraction, for entering it into the second stage with low-distortion. Besides the remaining error in the output $V(z)$ is the shaped quantization error $e_2(n)$ of the second-stage, operating with an input $e_1(n)$ which is itself noise-like, hence the second-stage quantization error $e_2(n)$ is very similar to a true white noise \([R6]\). In addition the MASH structure is very helpful for the use of a multi-bit quantizer in the second-stage, without any correction of the nonlinearity \([D2]\).

For example both stages are first-order loops, then:

$$\text{STF}_1 = \text{STF}_2 = 1 \quad \text{and} \quad \text{NTF}_1 = \text{NTF}_2 = 1 - z^{-1}$$

and the output is

$$V(z) = U(z) - (1 - z^{-1})^2 \cdot E_2(z)$$

This is identical to a single second-order $\Delta$-Σ modulator stated in equation (3-24).

Thus this MASH $\Delta$-Σ modulator has the noise-shaping performance of a second-order loop, while preserving the robust stability properties of first-order loops. Similarly for the second-order loops in both stages, then

$$\text{STF}_1 = \text{STF}_2 = 1 \quad \text{and} \quad \text{NTF}_1 = \text{NTF}_2 = (1 - z^{-1})^2$$

and the output is

$$V(z) = U(z) - (1 - z^{-1})^4 \cdot E_2$$

Thus this MASH $\Delta$-Σ modulator has the noise-shaping performance of a fourth-order loop, while preserving the robust stability properties of second-order loops.

Based on the useful MASH $\Delta$-Σ modulator, a two-stage $\Delta$-Σ DPWM with 11-bit resolution is proposed here. The proposed MASH $\Delta$-Σ DPWM is shown in Fig. 3-22 where both stages contain a first-order loop, resulting in a global second-order noise-shaping performance, while preserving the robust stability properties of first-order loops. In the 11-bit MASH $\Delta$-Σ DPWM, \(\text{STF}_1 = \text{STF}_2 = 1, \text{NTF}_1 = \text{NTF}_2 = (1 - z^{-1}), H_1 = \text{STF}_2, H_2 = \text{NTF}_1,\) and the output $V(z) = H_1 \cdot V_1(z) - H_2 \cdot V_2(z) = U(z) - (1 - z^{-1})^2 \cdot E_2(z)$, which is identical to equation (3.33). The 11-bit DPWM duty value from control algorithm is sent to the first-stage loop, and then 4-MSB for output and 7-LSB for error-feedback $e_1$. After the second-stage loop, the 2-MSB is delivered for output and 5-LSB for error-feedback $e_2$. Finally the 6-bit combination signals (4-MSB and 2-MSB) are sent to the hardware Core DPWM.
3.2.2 Operation of the Hybrid Δ-Σ DPWM Scheme

The 6-bit hardware Core DPWM is implemented by a 4-bit segmented DCM phase-shift block and a 2-bit counter-comparator which have been previously introduced in section 3.1.2 and section 3.1.3 respectively. Taking a combination of three blocks described above: MASH Δ-Σ modulator, 4-bit segmented DCM phase-shift block and 2-bit counter-comparator, the completed 11-bit hybrid Δ-Σ DPWM architecture can be figured in Fig. 3-23.

Similar to the operation of hybrid dither DPWM, the operation procedure of the hybrid Δ-Σ DPWM can be described as follows: The duty value $d$ is generated by the digital control law in 11-bit and varies from the minimum value $d[00000000000]$ (0) to the maximum value $d[11111111111]$ (2047), which is sent to the hybrid Δ-Σ DPWM architecture at beginning of each switching cycle. Initially, the 11-bit duty value $d$ goes into the MASH Δ-Σ modulator, where a new 6-bit duty value $D[5:0]$ is generated. For the new duty ratio $D$, the MSB $D[5:4]$ are delivered to the 2-bit counter-comparator block, and the LSB $D[3:0]$ are assigned for the 4-bit segmented DCM phase-shift block. The selected signals $S_c$ (from segmented DCM...
phase-shift block) and $S_k$ (from counter-comparator block) are operated by logic AND circuit, resulting in another signal $R_{set}$. The signals $S_{set}$ and $R_{set}$ respectively connect to the ports PRE and C of the FDP logic circuit to change the PWM states ON/OFF. For instance, supposing the $n$-cycle duty value from the control algorithm is $d(n) = "10010101010"b$, feedback value $e_1(n-1) = "0101010"b$ and $e_2(n-1) = "01010"b$ in the MASH Δ-Σ modulator, then the new duty $D(n) = "100101"b$ is generated. $D[5:4] = "10"b$ is implemented as the 2-bit counter comparator, $D[3:2] = "01"b$ is used to select phase-shifted clock $PX90$ for $S_1$, and $D[1:0] = "10"b$ is set to select phase-shifted clock $PY180$ for $S_2$. Through the logic AND operation of $S_1$ and $S_2$, the final phase-shifted signal $S_C$ is obtained and sent to FDP to change PWM signal. The logic waveforms for the example operation are shown in Fig.3-24.

In the FPGA implementation, the 11-bit digital PWM signal with 4MHz switching frequency is realized by the hybrid Δ-Σ DPWM architecture. Among the 11-bit DPWM, 5-bit are implemented as MASH Δ-Σ modulator ($N_{Δ,Σ} = 5$), 4-bit are achieved by segmented DCM phase-shift block ($N_{DCM} = 4$), and 2-bit are generated by counter-comparator ($N_{Core} = 2$). According to equations (3-16) and (3-17) respectively, the FPGA system clock is $F_{CLK} = 2^2 f_s$, and the clock signal shifted in DCM module is $F_{DCM} = 2^2 F_{CLK} = 2^4 f_s$. When operating at $f_s = 4$MHz the $F_{CLK}$ is merely 16MHz, which dramatically alleviates the clock requirement and can allow operation with low power consumption. For an example duty value of $D[5:0] = "100011"b$ in FPGA implementation, the timing-simulation waveforms of the 4-bit segmented DCM phase-shift is shown in Fig. 3-25, and the waveforms of the complete 11-bit hybrid Δ-Σ DPWM is shown in Fig. 3-26. The experimental tests of the hybrid Δ-Σ DPWM based on a discrete buck converter will be detailed in Chapter 6.
3.3 Summary

To improve the output voltage precision, the resolution of the ADC and DPWM is expected to the higher the better. Based on the hardware Core DPWM, the effective resolution of the DPWM architecture can be boosted with soft methods as digital dither and delta-sigma, allowing for high-frequency, low-power and small-area implementations. A summarization for the two types of hybrid DPWM is given by Table 3-5.

The hybrid dither DPWM includes the digital dithering approach and the hardware Core DPWM. The bit number of dither \( N_{dib} \) can be determined according to useful analysis in part B of section 3.1.1. However dither is not coming free. The more bits of dither, the more additional ripple will occur. Whatever the soft method dither is valuable to increase the effective DPWM resolution to support operation at higher frequency than 1MHz with 11-bit effective resolution, which is impractical for most of pure hardware DPWM.

The hybrid \( \Delta - \Sigma \) DPWM uses the noise-shaping technique to increase DPWM resolution
while consuming less power and area in higher frequency range. Although Δ-Σ architecture has been used for years in the design of ADC and DAC that can be implemented with low cost CMOS technologies, it is still rarely applied to the DPWM design in digital controller for high-frequency low-power SMPS. There are several reasons accommodating this. Firstly there is lack of understanding in the design of Δ-Σ DPWM principle by power-supply engineers. No systematic procedure is available for the design of Δ-Σ DPWM. Secondly there are seldom discussions regarding the usefulness and advantages of Δ-Σ DPWM in theoretical, not to mention the practical implementation proven. Thirdly due to absence of standard criterion for NTF properties that are necessary and sufficient for stable operation, it is difficult to exactly estimate the stability of a high-order Δ-Σ modulator. If we have standard criterions to solve this stability problem of a high-order Δ-Σ as well as the guarantee minimum-ripple digital dither, the Δ-Σ modulator will be a huge potential in DPWM application for digitally controlled SMPS.

As alternative methods, the two proposed Hybrid DPWMs evidently offer higher-frequency and higher-resolution operation. However it does not have enough proof to evaluate their performance and prove which one is better. When DPWM applied to practical implementation, the consideration of hardware resources, power consumption and output voltage accuracy, etc should be carefully taken into account.

This chapter discussed the digital PWM implementation of a switching converter, and presents two kinds of high resolution hybrid DPWM design. The next chapter will detail the design of digital control law as classical PID and robust RST controllers.

<table>
<thead>
<tr>
<th>symbol</th>
<th>Definition</th>
<th>Hybrid dither DPWM</th>
<th>Hybrid Δ-Σ DPWM</th>
</tr>
</thead>
<tbody>
<tr>
<td>$N_{DPWM}$</td>
<td>Bit number of DPWM effective resolution</td>
<td>11-bit $d[10:0]$</td>
<td>11-bit $d[10:0]$</td>
</tr>
<tr>
<td>$N_{Core}$</td>
<td>Bit number of counter-comparator</td>
<td>4-bit $d[10:7]$</td>
<td>2-bit $d[10:9]$</td>
</tr>
<tr>
<td>$N_{phase-shift}$</td>
<td>Bit number of segmented DCM</td>
<td>4-bit $d[6:3]$</td>
<td>4-bit $d[8:5]$</td>
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<tr>
<td>$N_{soft}$</td>
<td>Bit number of soft method (dither or Δ-Σ)</td>
<td>3-bit $d[2:0]$ ($N_{dith}$)</td>
<td>5-bit $d[4:0]$ ($N_{Δ-Σ}$)</td>
</tr>
<tr>
<td>$f_s$</td>
<td>Operation switching frequency in FPGA</td>
<td>Up to 2MHz</td>
<td>Up to 4MHz</td>
</tr>
<tr>
<td>$f_{CLK}$</td>
<td>System clock for hardware Core DPWM</td>
<td>$2^{N_{Core}} \cdot f_s = 32$MHz</td>
<td>$2^{N_{Core}} \cdot f_s = 16$MHz</td>
</tr>
<tr>
<td>$f_{DCM}$</td>
<td>Phase-shift clock inside DCM block only</td>
<td>$2^{N_{Core}+2} \cdot f_s = 128$MHz</td>
<td>$2^{N_{Core}+2} \cdot f_s = 64$MHz</td>
</tr>
</tbody>
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